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1 [Algorithms and data structures for flash memories](#)

Eran Gal, Sivan Toledo

June 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 2

Publisher: ACM Press

Full text available: [pdf\(343.39 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Flash memory is a type of electrically-erasable programmable read-only memory (EEPROM). Being nonvolatile and relatively dense, they are now used to store files and other persistent objects in phones, digital cameras, portable music players, and many other computer systems in which memory is inappropriate. Flash, like earlier EEPROM devices, suffers from two limitations. First, bits can only be programmed on a large block of memory. Second, ...

Keywords: EEPROM memory, Flash memory, wear leveling

2 [Hardware Engines for Bus Encryption: A Survey of Existing Techniques](#)

R. Elbaz, L. Torres, G. Sassatelli, P. Guillemin, C. Anguille, M. Bardouillet, C. Buatois, J. B. Rigaud
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - VLSI**
Publisher: IEEE Computer Society

Full text available: [pdf\(194.68 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

The widening spectrum of applications and services provided by portable and embedded devices raises concerns in security. Most of those embedded systems (pay-TV, PDAs, mobile phones, etc...) must exchange data with the outside world. As a result, the main problem is that data and instructions are constantly exchanged between the device and the outside world in clear form on the bus. This memory may contain confidential data like commercial software or personal data of the end-user or the company.

3 [GPGPU: general purpose computation on graphics hardware](#)

 David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Alan F. Sellen
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**
Publisher: ACM Press

Full text available: [pdf\(63.03 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#)

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful processor. The latest graphics architectures provide tremendous memory bandwidth and computation power. They feature fully programmable vertex and pixel processing units that support vector operations up to full floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible to a wide range of applications.

GPUs are highly parallel s ...

4 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyen
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Publisher: ACM Press

Full text available:  [pdf\(2.96 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

This paper compares eight commercial parallel processors along several dimensions. The processors include multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the Alliant FX2) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper analyzes the computers from the standpoint of interconnection structures, memory configurations, and instruction sets. Also, the share ...

5 Architectural Support for High Speed Protection of Memory Integrity and Confidentiality in Large Systems

Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu

September 2004 **Proceedings of the 13th International Conference on Parallel Architecture and Compilation Techniques PACT '04**

Publisher: IEEE Computer Society

Full text available:  [pdf\(255.33 KB\)](#)

Additional Information: [full citation](#), [abstract](#)

Recently there is a growing effort in both the architecture and the security community to create mechanisms for authenticating system memory. As shown in the previous work, hardware-based memory authentication is a key component for creating future trusted computing environments and digital rights protection. All previous work has been focused on authenticating memory exclusively owned by a single processing element. However, in real-world platforms, memory is often ...

6 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(385.22 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This tutorial surveys design methods for energy-efficient system-level design. We consider energy efficiency at the system level, which includes both hardware and software layers. We consider the three major constituents of hardware energy consumption: computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software. This survey ...

7 Cryptography as an operating system service: A case study

Angelos D. Keromytis, Jason L. Wright, Theo De Raadt, Matthew Burnside

February 2006 **ACM Transactions on Computer Systems (TOCS)**, Volume 24 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(669.12 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Cryptographic transformations are a fundamental building block in many security applications and, to support this performance, several vendors market hardware accelerator cards. However, until now no operating system provided a mechanism that allowed both uniform and efficient use of this new type of resource. We present the Open Cryptographic Framework (OCF), a service virtualization layer implemented inside the operating system kernel that provides uniform access to accelerator functions ...

Keywords: Encryption, authentication, cryptographic protocols, digital signatures, hash functions, security, operating systems, virtualization, cryptography

8 Forth: Ten years of Forth in ACM Sigplan Notices: part 2

Paul Frenger

April 2006 **ACM SIGPLAN Notices**, Volume 41 Issue 4

Publisher: ACM Press

Full text available:  [pdf\(268.55 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index term](#)

Last column, we began a two-part retrospective to recap the first ten years of the *ACM Sigplan* walk through memory lane began with a history lesson: who Chuck Moore is, the origins of the Forth software and hardware incarnations, some vendors, conferences, and a few tall tales. We *SIG-Forth* and its four-year *Newsletter*, and how phoenix-like their ashes gave rise to the ten-y

9 Power reduction techniques for microprocessor systems

Vasanth Venkatachalam, Michael Franz

September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3

Publisher: ACM Press

Full text available:  [pdf\(602.33 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index term](#)

Power consumption is a major factor that limits the performance of computers. We survey the " that reduce the total power consumed by a microprocessor system over time. These techniques ranging from circuits to architectures, architectures to system software, and system software to include holistic approaches that will become more important over the next decade. We conclude a ...

Keywords: Energy dissipation, power reduction

10 RAID: high-performance, reliable secondary storage

Peter M. Chen, Edward K. Lee, Garth A. Gibson, Randy H. Katz, David A. Patterson

June 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 2

Publisher: ACM Press

Full text available:  [pdf\(3.60 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [similar](#)

Disk arrays were proposed in the 1980s as a way to use parallelism between multiple disks to improve performance. Today they appear in the product lines of most major computer manufacturers. This comprehensive overview of disk arrays and provides a framework in which to organize current research. This article introduces disk technology and reviews the driving forces that have popularized disk arrays. It discusses the two ...

Keywords: RAID, disk array, parallel I/O, redundancy, storage, striping

11 Special issue: AI in engineering

D. Sriram, R. Joobbani

April 1985 **ACM SIGART Bulletin**, Issue 92

Publisher: ACM Press

Full text available:  [pdf\(8.79 MB\)](#)

Additional Information: [full citation](#), [abstract](#)

The papers in this special issue were compiled from responses to the announcement in the July newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the number of papers received from over six countries. About half the papers were received over the computer network.

12 MANTIS OS: an embedded multithreaded operating system for wireless micro sensor platforms

Shah Bhatti, James Carlson, Hui Dai, Jing Deng, Jeff Rose, Anmol Sheth, Brian Shucker, Charles Giannino, Richard Han

August 2005 **Mobile Networks and Applications**, Volume 10 Issue 4

Publisher: Kluwer Academic Publishers

Full text available:  [pdf\(1.27 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index term](#)

The MANTIS MultimodAI system for NeTworks of In-situ wireless Sensors provides a new multi-level embedded operating system for wireless sensor networks. As sensor networks accommodate in-network compression/aggregation and signal processing, preemptive multithreading in the MANTIS system allows micro sensor nodes to natively interleave complex tasks with time-sensitive tasks, thereby mitigating the producer-consumer problem. To ac ...

Keywords: cross-platform, dynamic reprogramming, embedded operating system, lightweight, sensor networks

13 The Alpha demonstration unit: a high-performance multiprocessor

◆ Charles P. Thacker, David G. Conroy, Lawrence C. Stewart
◆ February 1993 **Communications of the ACM**, Volume 36 Issue 2

Publisher: ACM Press

Full text available:  [pdf\(6.26 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index term](#)

Keywords: Alpha AXP chip

14 Burroughs Corporation: corporate public relations

◆ October 1974 **ACM SIGMICRO Newsletter**, Volume 5 Issue 3

Publisher: ACM Press

Full text available:  [pdf\(7.37 MB\)](#)

Additional Information: [full citation](#)

15 The evolution of the DECsystem 10

◆ C. G. Bell, A. Kotok, T. N. Hastings, R. Hill
◆ January 1978 **Communications of the ACM**, Volume 21 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(1.92 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index term](#)

The DECsystem 10, also known as the PDP-10, evolved from the PDP-6 (circa 1963) over five generations of implementations to presently include systems covering a price range of five to one. The origins of the operating system, and languages are described in terms of technological change, user requirements, and costs. The PDP-10's contributions to computing technology include: accelerating the transition from batch processing to timesharing; ...

Keywords: architecture, computer structures, operating system, timesharing

16 Personal distributed computing: the Alto and Ethernet hardware

◆ Chuck Thacker
◆ January 1986 **Proceedings of the ACM Conference on The history of personal workstations**

Publisher: ACM Press

Full text available:  [pdf\(1.69 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index term](#)

Between 1972 and 1980, the first distributed personal computing system was built at the Xerox PARC. The system was composed of a number of Alto workstations connected by an Ethernet local network that provided centralized facilities. This paper describes the development of the hardware that made the system possible.

17 Neon: a single-chip 3D workstation graphics accelerator

Joel McCormack, Robert McNamara, Christopher Ginos, Larry Seiler, Norman P. Jouppi, Ken Corcoran
August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics Hardware**



Publisher: ACM Press

Full text available: [pdf\(1.58 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: chunk rendering, direct rendering, graphics pipeline, level of detail, rasterization, texture mapping, vertex shading

18 PicoDBMS: Scaling down database techniques for the smartcard

Philippe Pucheral, Luc Bougnim, Patrick Valduriez, Christophe Bobineau

September 2001 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 17 Issue 3

Publisher: Springer-Verlag New York, Inc.

Full text available: [pdf\(259.03 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

Smartcards are the most secure portable computing device today. They have been used successfully in banking, healthcare, insurance, etc. As smartcards become more powerful (with 32-bit CPU and more than 1 MB of stable memory in the next versions) and become multi-tasking devices, the need for database management arises. However, smartcards have severe hardware limitations (very slow processor, constrained stable memory, etc.).

Keywords: Atomicity, Durability, Execution model, PicoDBMS, Query optimization, Smartcard, Transaction processing

19 1 - Special Section: Efficient software implementation of embedded communication protocols

◆ asynchronous software thread integration with time- and space-efficient procedure calls

Nagendra J. Kumar, Vasanth Asokan, Siddhartha Shivshankar, Alexander G. Dean

February 2007 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 6 Issue 1

Publisher: ACM Press

Full text available: [pdf\(596.75 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The overhead of context switching limits efficient scheduling of multiple concurrent threads on a single processor. If the time requirements exist, a software-implemented protocol controller may be crippled by this problem. If the time requirements are too short to recover through context switching, so only the primary thread can execute during the time of the secondary threads and potentially missing deadlines. Asynchronous software thread integration provides a solution to this problem.

Keywords: Asynchronous software thread integration, J1850, fine-grain concurrency, hardware-implemented communication, hardware-implemented communication protocol controllers

20 Cache memory performance in a unix environment

◆ Cedell Alexander, William Keshl, Furrokh Cooper, Faye Briggs

June 1986 **ACM SIGARCH Computer Architecture News**, Volume 14 Issue 3

Publisher: ACM Press

Full text available: [pdf\(2.10 MB\)](#)

Additional Information: [full citation](#), [citations](#), [index terms](#)

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